Three-terminal Ballistic Junctions as Building Blocks for Nanoelectronic Devices

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A three-terminal ballistic junction (TBJ) is a device in which three quantum point contacts (or electron waveguides) are coupled via a ballistic region [1]. Theoretical and experimental studies [1-5] have shown that the TBJs exhibit a novel electrical property which has potential applications in nanoelectronics, such as rectification, harmonic generations, and logic functions. The modeling has also shown that the effect is observable at room temperature, it is robust against asymmetry, and it does not depend on the angle between the left and right branches of the TBJ [1]. Here, based on our recent investigations, we will demonstrate that various nanoelectronic devices can be fabricated using the TBJs as building blocks. In particular, the results of our recent design, fabrication, modeling and measurements of TBJ diodes and transistors, TBJ frequency multipliers, and TBJ logic gates will be presented and discussed.

The results of experiments to be presented have mainly been obtained based on devices made from high-quality InGaAs quantum well materials, but the properties of the devices have also been observed in experiments with other herterostructure materials. Figure 1(a) shows an SEM image of a typical T-shaped TBJ device made from GaInAs/InP quantum well system using electron beam lithography and wet chemical etching. The dimension of the active area of the devices is about 200 nm. The measured electron mean free path in this quantum-well material varies from a few microns at 0.3 K to ~ 130 nm at room temperature. Thus, the electron transport in our devices is expected to be ballistic or quasi-ballistic up to room temperature. The characteristics of the output voltage V_C as a function of V, with $V_L = V$ and $V_R = -V$, were measured. The obtained results are compared with the prediction of Ref. [1] and a good agreement is found. Furthermore, room-temperature diode and triode behaviors of the TBJs as predicted in Ref. [4] were experimentally demonstrated [see Fig. 1(b)].

Several integrated devices designed by using TBJs as building blocks were also fabricated and characterized. As an example, we show a TBJ-based logic device that was made by integration of a T-shaped TBJ and a point contact on high-mobility GaInAs/InP quantum well materials. The $4 \times 4 \mu m^2$ scanning electron microscope image of the device and the measurement circuit setup are shown in Fig. 2(a). The output voltage measured at room temperature as a function of the two input voltages is shown in Fig. 2(b). It can be seen that the device performs the logic NAND function. It can also be seen that the device has a gain, i.e., the amplitude of the output voltage is larger than the amplitude of the input voltages. In addition, this device, in the present circuit configuration, can also be used as a frequency multiplier. Several other functional and logic devices have also been designed with the TBJs as building blocks and have been fabricated and characterized.

To conclude, the TBJs have been fabricated and characterized. Various functional devices, such as frequency multipliers and logic gates, designed with the TBJs as building blocks have been realized. We emphasize that all these devices with potential applications in nanoelectronics can be fabricated with ultrasmall dimensions by a single-step lithography process and function at room temperature.

References

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Figure 1: (a) AFM image of a T-shaped TBJ fabricated from high-mobility GaInAs/InP quantum well material. The lithographic widthes of the three branches in the TBJ are about 200 nm. (b) Measured room-temperature triode behavior of the T-shaped TBJ as shown in (a). Here the output voltage, V_C , from the central branch is plotted as a function of the voltage, V_L , applied to the left branch, for various voltages, V_R , applied to the right branch.



Figure 2: A TBJ-based NAND logic gate made by lateral integration of a T-shaped TBJ with a point contact on high-mobility GaInAs/InP quantum well system. (a) shows an SEM image of the device and the schematic diagram of the measurement circuit. (b) shows the measured output signal vs the two input signals for the circuit setup shown in (a) at room temperature.