Two-Dimensional Metallic State in Silicon-on-Insulator Structures

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The metallic state of a two-dimensional (2D) electron gas in silicon-on-insulator structures possesses similar properties to that of high-mobility Si-metal oxide structures (MOS). It shows the characteristic resistance drop towards low temperatures and a strong increase with parallel magnetic fields [1].

So far the maximum carrier mobility in SOI structures was clearly below that of the best Si-MOS ones. Now new SOI structures reach a maximum electron mobility of 25,000 cm^2/Vs – a value comparable to many investigated high-mobility Si-MOS structures in the literature. The SOI-MOS samples were fabricated on commercially available bonded SOI wafers with 100 nm SOI layer and 400 nm buried oxide. After the processing steps the final SOI film thickness was 40 nm. The gate oxide was 40 nm thick and the gate material was 200 nm thick phosphorus doped poly-Si film.

The behavior of the metallic state in our new SOI structures shows several differences to earlier investigated Si-based structures. At high densities, the resistivity drop versus temperature is similar to typical Si-MOS structures. But at lower densities, the resistivity first shows a pronounced drop towards lower temperature followed by a strong increase below about 1 K (see Fig. 1). The non-monotonic behavior of the resistivity reflects probably the contribution of two different mechanisms like coherent conductivity corrections in the ballistic regime and the strong localization effect. The experimentally observed behavior will be compared with a detailed analysis of the possibly contributing effects.

In the regime, where the SOI sample changes the behavior at low temperature from metallic to insulating, we further found a reproducible non-monotonic behavior of the longitudinal resistivity ρ_{xx} versus the applied gate voltage V_g. A typical scan of $\rho_{xx}(Vg)$ is shown if Fig. 2 with high resolution. The full curve represents the gate voltage sweep from high (1 V) to low (0.5 V) voltage, whereas the small points show the measurement where V_g was varied in the other direction. These fluctuations vanish between approximately 1 and 2 K. It is not clear at the moment whether the fluctuations are caused by processes inside the bulk 2D layer or if they are generated in the contact regions. Correspondingly, the fluctuations may be caused by recharging of trap states or by coherent electron diffusion in the potential landscape, i.e. universal conductance fluctuations. The origin of the reproducible fluctuations will also be studied in detail.

(See figures on page 2.)

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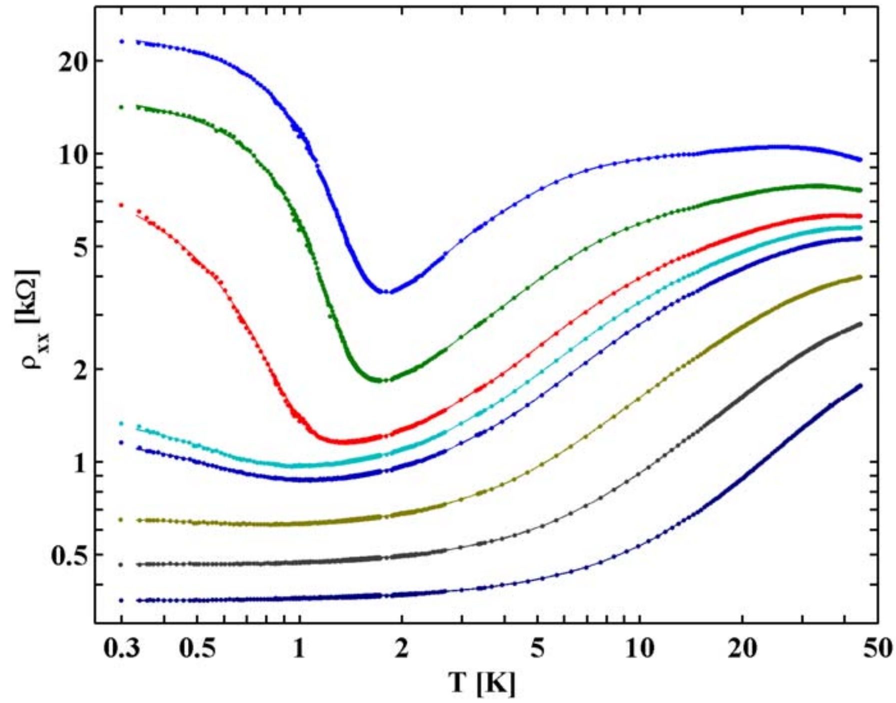

Fig. 1: Longitudinal resistivity ρ_{xx} versus temperature T for SOI sample N1SB-E4-8. The electron density corresponds to 1.45, 1.92, 2.40, 2.63, 2.87, 3.82, 5.24, and 7.61 x 10^{11} cm^{-2} from top to bottom traces.

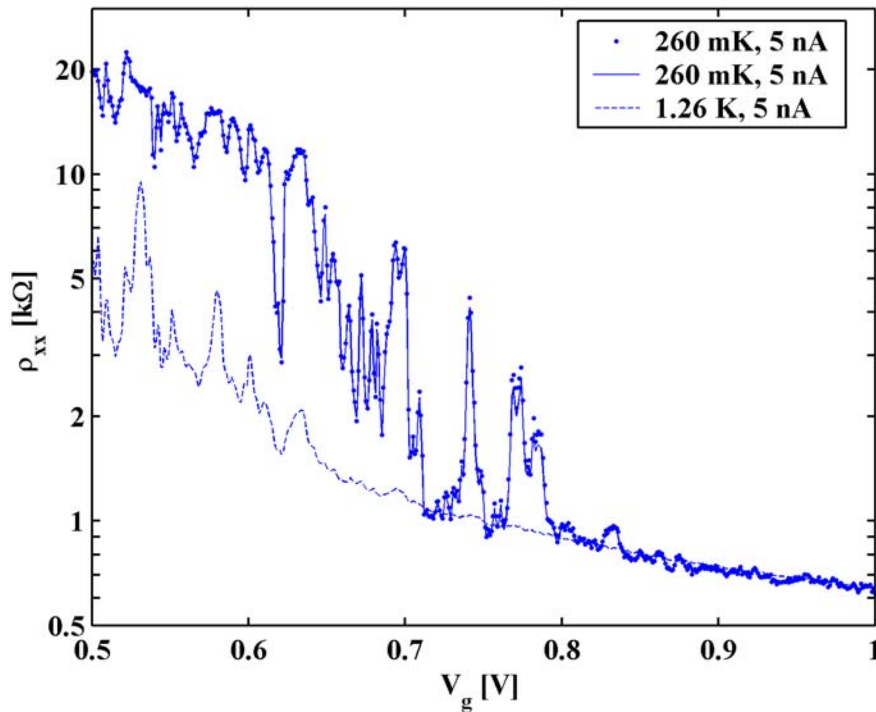

Fig. 2: Longitudinal resistivity ρ_{xx} versus gate voltage V_g. The full line represents a measurement from Vg = 1 V down to 0.5 V and the dots show the reverse measurement from low to high Vg at T = 260 mK and a measurement current of 5 nA. The dashed line represents a measurement at an elevated temperature of 1.26 K. The presented V_g range corresponds to an electron density of 1.45 to 3.82 x 10^{11} cm^{-2}.